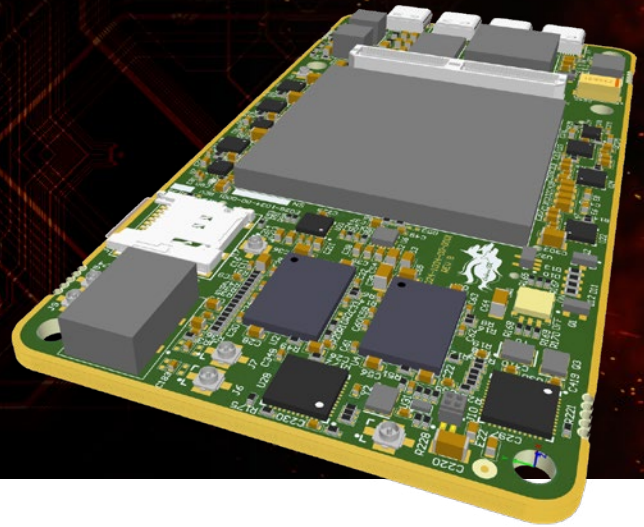




Cerberus Radio

**16 TX/RX Channels, Smallest Footprint
Software Defined Radio/RADAR**



DIGITAL SIGNAL PROCESSING HORSEPOWER

Multi-processor Subsystem

Xilinx 16nm FinFET RFSoc XCZU29

Quad core 1.2 GHz ARM Cortex-A53 64b with L1/L2, MMU, DMA

Dual 500MHz R5 real time processor, power manager & secure boot

4GB DDR4, Micro SD memory

Range of IO including UARTs, 1G Ethernet, USB3.0

Massive parallel AXI IO between PS and FPGA fabric

FPGA Resources

930+ system logic cells (K), 16 32g SERDES

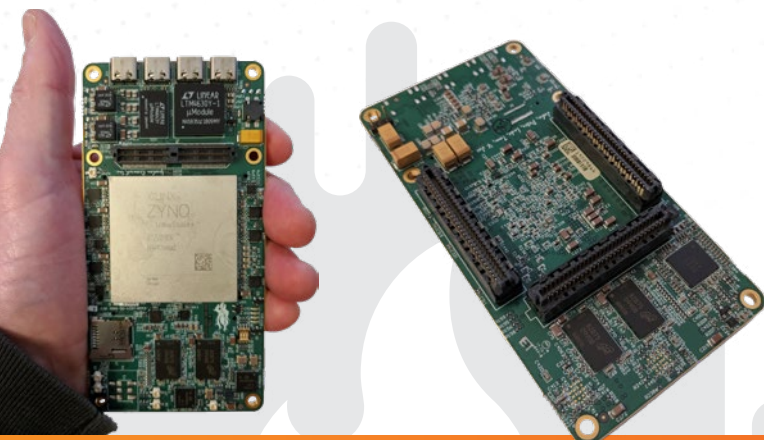
4,272 DSP slices, 2.13 TMACs @ 500 Mhz

MADE FOR SMALL FORM FACTOR AIRBORNE RADIO

Small Form Factor 122mm X 62mm x 10mm envelope

6V-16V input voltage

Typical power ~38W, depends on software & DSP work load



RF TRANSCEIVER FRONT END

RF Front End

TX and RX RF range 0 to 4 GHz (frontend analog bandwidth)

16 Differential 12-bit ADC Channels up to 2 GSPS (1GHz BW)

16 Differential 14-bit DAC Channels up to 6 GSPS

Phase Coherent Clocking Scheme

Clock Subsystem Supports Multiple Cerberus Phase Synchronization

Digital Front End

Digital Bandpass Filter per Channel

Quadrature Error Correction for TX & RX paths (gain/phase/offset)

48-bit Fractional-N digital NCO & mixer per converter

Expandable and Scalable

Board to board expansion connector with up to 32GB data transfer

2 Cerberus modules plugs into Hydra 400GbE (4 x 100GbE optical links)

Future GNU RADAR Tiling adapter, 5.8GHz RF, and flat panel antenna

Clock Distribution Subsystem

122.88MHz VCXO, custom reference clocks available

External Inputs: clock reference & 1PPS & SYSREF (phase sync)

Generates all ADC/DAC/Synth clocks & SYSREF

